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A REVIEW ON ULTRA LOW VOLTAGE LOW NOISE AMPLIFIER USING ACTIVE INDUCTOR FOR ULTRA WIDEBAND APPLICATION

Mileshwar sinha(M.Tech student)[1]
Electronics and telecommunication
SSGI (FET), JUNWANI ROAD
BHILAI (C.G.), India
milesh83@gmail.com

Asst. Prof. Khemraj desmukh[2]
Electronics and telecommunication
SSGI (FET), JUNWANI ROAD
BHILAI (C.G.), India
khemraj.desmukh@gmail.com

Abstract: — during this paper we tend to discuss a unique design of CMOS low noise electronic equipment (LNA) for the applying of low voltage RF circuit employed in radical wide band application. we tend to addressing a replacement methodology to optimize the circuit parameter like power potency, noise figure (NF) and improved methodology of input and output matching. Comparison among the LNA square measure drained terms of gain, noise figure, linearity, stability and style strategy of electrical device. This paper offers the thought to the longer term analysis to style higher LNA in terms of low power consumption, stability and higher vary of frequency of operation.

Keywords—CMOS, IC (Integrated circuit), LNA (low noise amplifier) low power, linearity, low voltage, RF (radio frequency), stability, UWB (ultra wide band).

I. INTRODUCTION

In RF CMOS technology the most important difficulties of RF CMOS circuit implementation square measure power consumption, poor noise performance and unity gain frequency of CMOS technology. This successively shrinks down IC each in terms of space and power provide. Thus the ICs square measure needed to be style in deep submicron technology with low voltage and power provide. The larger drawback is that the lack of systematical style approach for RF CMOS circuit implementation. This reported radical wide band (UWB) CMOS LNA style may be found in [1]. The LNA introduce in [1] employs series inductive peaking within the feedback circuit is analyzed and used to reinforce the information measure and noise performance of LNA. Another general approach permitting low noise electronic equipment with out-bands rejection topology by victimization changed low noise active electrical device [2]. Because the low noise electronic equipment is extremely initial stage of the receiver. Here during this paper we tend to proposes a large band input network without-band rejection capability to suppress the out-band properties as its initial stage of LNA. During this paper we tend to propose a sensible methodology of CMOS LNA style for UWB application with relation to ohmic resistance matching and power/noise improvement.

The FFC (federal communication commission) in USA has approved an oversized information measure of 7GHz from three.1GHZ to 10.6 GHz for business application of radical wide band technology [3]. On increase the info rate up to 480Mb/s and low power provide. This is often substantially essential reason for the UWB wireless application. during this paper a coffee power associate degree high gain UWB LNA with forward body bias technique for low voltage operation is mentioned to extend the gain of the circuit 2 stage LNA common supply sort is employed.

II. TRADITION OF LNA CIRCUIT SYNTHESIS

The first basic amplifier models which are used in LNA are common source, common drain and common gate amplifier. In most of the LNA common source amplifier is used as it gives the high gain factor as compare to CD and CG, stability and linearity. Common drain amplifier is used for the buffer stage of LNA and CG is used for the cascading of LNA [1]. In the proposed work inductive source degenerated topology of common source amplifier is to be used. As shown in figure this give the maximum power gain by trying to minimize feedback effect which mainly scarifies the gain of circuit [2]-[3].

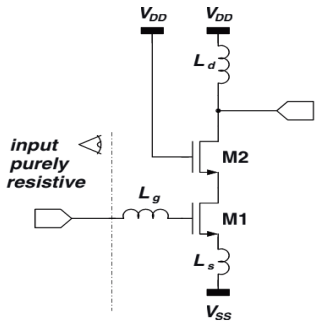

Fig. 1 basic CS amplifier to inductive degenerated CS LNA

The most popular topology for implementation of the LNA circuit with enhanced gain performance feature is cascode configuration [3]. A series peaking inter stage inductor Lx with a cascode circuit is show in fig. 2 where impedance Zx is seen above the drain of input CS stage and can be calculated as [3]

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$$Zx \approx sLx + \frac{1/gm2}{1+s(ci2/gm2)} \quad (1)$$

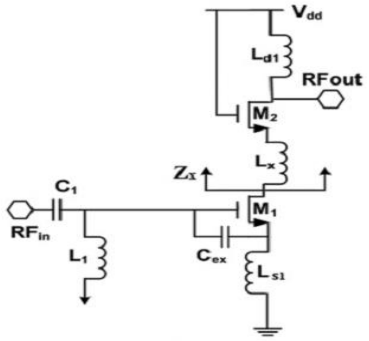

Fig. 2 schematic of traditional cascode CS LNA

Where,

gm2 = transconductance of cascode transistor M2

C2 = total input capacitance at the source node of M2

In this configuration, cascode can be considered as a combination of two cascode amplifier, where M1 is the first stage CS amplifier followed by M2 common gate amplifier. For proper operation of cascode circuit, stacked transistors must operate in the saturation region. Because of stacked architecture, cascode circuit requires a high Vdd, where Vdd is limited to 2*Vdsat [3]. And can increase overall power consumption of the cascode circuit. The resulting issue can be resolved by reducing width of both the transistor, but this solution still affects other LNA FOMs, such as, noise, gain, input matching and Si area. To understand these issues in an effective manner, we explain cascode topology shown in Fig. 2 The total voltage gain (GF) of the cascode topology can be derived as

$$G_F = -gm1 \frac{1}{(1+sZxC_{01})} \frac{1}{(1+s(Ci2/gm2))} \quad (2)$$

It is clear from (2) that the voltage gain of cascode topology has a pole at

$$f0 = \frac{gm2}{2\pi Ci2} \quad (3)$$

Because of Lx, Zx shows inductive nature and resonates with total output parasitic capacitance Co1 at high frequency, resulting a peak in gain response. In absence of an inter-stage inductor Lx, simulation results show a gain roll-off problem in the mid-frequency region (6– 14 GHz). Although, both the gain and NF improves, when an inter-stage inductor Lx is introduced in the cascode topology. However, the roll-off problem still appears in this frequency region because of mismatch in the input return loss. The inductor Lx is chosen to increase the gain, so that, noise of the cascode topology can be reduced. Mismatch in the input return loss is a major reason for the gain roll-off, which confirms a trade-off between gain and input matching. To further improve the gain as well as to overcome the gain roll-off, if we cascade additional CS stages with the cascode circuit, it will increase the gain, but at the cost of increased Si chip area.

III. LNA DESIGN CONSIDERATION

A. Transister Scaling And Biasing Condition

Since the size of transistor and bias condition determine the power dissipation, it is often recommended to decide them with a certain power budget. However, we should evaluate the size of the transistor versus bias condition carefully, because they are also related to the impedance seen by the input gate. Thus, the first choice is to determine the size and bias condition that satisfies both impedance and noise matching with limited bias current. According to the MOSFET noise analysis [3], the generator (sometimes source) admittance for optimal noise performance is given by (4.1) and (4.2).

$$G_{opt} = \alpha\omega C_{gs}\sqrt{\frac{\delta}{5\gamma}(1-|c|^2)} \quad (4.1)$$

$$B_{opt} = -\omega C_{gs}\left(\left(1+\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)\right. \quad (4.2)$$

Where $\alpha = gm/gds0$, and noise parameters c, δ, and γ as defined in [4].

For the sake of simplicity, we ignore the correlation of noise so that c can be set to 0. Therefore, we can simplify (4.1) and (4.2) as,

$$R_{opt} \approx \frac{1}{\alpha\omega Cgs}\sqrt{\frac{5\gamma}{\delta}} \quad (5.1)$$

$$X_{opt} \approx \frac{1}{\omega C_{gs}} \quad (5.2)$$

Furthermore, by taking into account the degenerative inductor Ls at the source-end, (5.2) can be modified as

$$X_{opt} \approx \frac{1}{\omega C_{gs}} - \omega Ls \quad (5.3)$$

It is clear that optimal noise condition and maximum power delivery are obtained simultaneously when Zopt=Zin_eq*, where Zin_eq is the equivalent input impedance seen by input gate of amplifying transistor given by

$$Z_{in\_eq} = R_{in\_eq} + jX_{in\_eq} = \frac{gmLs}{C_{gs}} + j\left(\omega Ls - \frac{1}{C_{gs}}\right) \quad (6)$$

However, since it is not easy to make both Zopt and Zin_eq* equal, thus it better satisfies the inequality as shown in (7) for higher gain. Obviously, smaller resistive term of input impedance seen by the gate-end leads to higher gain [4].

$$Rin\_eq \leq Ropt \leq Rs \quad (7)$$

Where, R_s is the resistive term of source impedance Z_s.

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Since electrical phenomenon term of Zopt and Zin_eq* area unit nearly always matched in line with (5.3) and (6), difference (7) can force Zin_eq to make a much bigger circle than Zopt within the Smith chart illustration for the frequency vary of interest. As mentioned already, we have a tendency to verify a bias condition with limiting bias current so DC bias current IDS could be a fastened worth. For simplicity, we have a tendency to assumed g = μnCox (W/L) Veff and Cgs system = (2/3)WLCox by ignoring overlapped channel length Lov, Associate in Nursing these provide an initial Veff as in (8).

$$\text{Veff} \leq \frac{2\text{RsL}^2}{3\text{Ls}\mu\text{n}} \qquad (8)$$

Note that we have a tendency to area unit considering minimum channel length *L*in (8). Once we have a tendency to verify the most Veff, we are able to specify the minimum *gm* as *gm ≥ 2IDS/Veff_max*, wherever *Veff_max* is that the most effective voltage.

Assuming $\gamma \approx 2$, $\delta \approx 4$, and $\alpha \approx 5$ as a result of $g_{ds} \approx 0.2g_m$ in active region, (5.1) will be any simplified as $\text{Ropt} \approx 1/\sqrt{10}\omega\text{Cgs}$. Thus, we can determine a minimum channel breadth *W* as $\text{W} \geq 3/2\sqrt{10}\omega\text{RsLCox}$. Again, minimum channel length is assumed [4].

B. Input Impedance Matching

For band electrical resistance matching, we've got to transfer the supply electrical resistance Z_s, that is generally $Z_s = R_s = 50\ \Omega$, to *Zin_eq** over the frequency vary of interest. Conjugate matching can satisfy the best noise condition and electrical resistance matching at the same time as a result of electronic transistor size and bias condition represented earlier.

First, we have a tendency to derive the first order Butterworth type bandpass filter from a low pass filter image that has been terminated with R_{in_eq} at each the ends, as shown in Figure 3. In Figure 3, ω_c is the center frequency of the target frequency varies at outline as $\omega_L + (\omega_H - \omega_L)/2 = \omega_L + BW/2$ and *BW* is the bandwidth that the information measure needed for the target circuit. Note that ω_H and ω_L are the higher and lower stop frequencies respectively. Parameter *r* is defined by ω_c/BW. Since we have a tendency to have an interested in signal reflection and not the 3dB bandwidth, the middle frequency is chosen as ω_c, not like the general band pass filter development procedure [5] that defines $\omega c = \sqrt{\omega_H \omega_L}$.

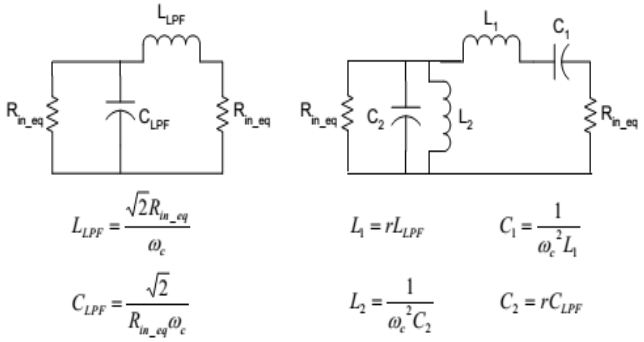

Fig. 3 frequency transformation

The band pass filter synthesized with the middle frequency ω_c has minimum power reflection at the center frequency in order that it satisfies the electrical phenomenon impedance match over the complete target bandwidth at the value of small gain reduction in the higher frequency range.

Obviously, C_1 and L_1 is comparable to C_{gs} and L_s+L_g severally, wherever L_g is that the further inductor connected to gate. Expressions L_{LPF}, C_1 and L_1 in Figure 3 will confirm the selection of L_s as

$$L_s \geq \frac{BW_{\min}}{\sqrt{2}\omega_c^2 g_m} \qquad (9)$$

Where BW_{min} is the minimum needed bandwidth.

By definition, the power loss over the stop band is about 3dB. However, 3dB power loss is unacceptable in terms of power reflection and hence 50% excessive bandwidth is suggested to ensure an S11 of –10dB over the frequency band of interest. Since our target band is 3*GHz* to 5*GHz*, we have a tendency to apply 2*GHz* to 6*GHz* bandwidth with the fixed center frequency of 4*GHz*. Once we design a bandpass filter with R_{in_eq} terminated at both the ends, R_{in_eq} at the input side should be transferred to Z_s with an impedance inverter as shown in Figure 4.

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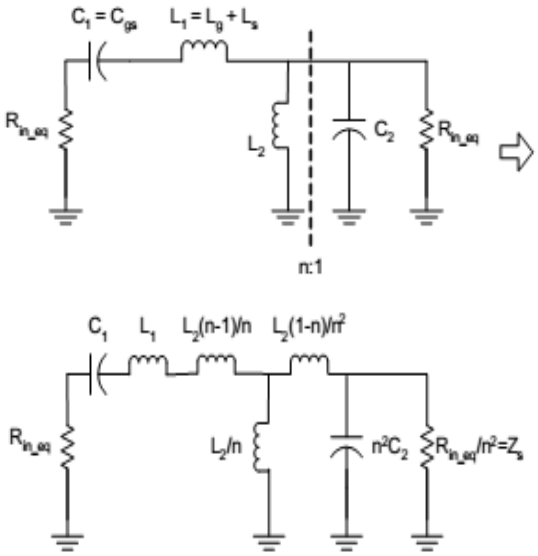

Fig. 4 Impedance inverting

Since we adjusted the R_{in_eq} to be smaller than Z_s, inverting factor n in Figure 4 is smaller amount than unity, in order that the inductance $L_2(n-1)/n$, which is connected to L_1 in series, may be a negative value leading to a smaller gate inductance L_g. In general, R_{in_eq} isn't very small when compared to Z_s, therefore n is incredibly near to unity as per to the definition $n = \sqrt{R_{in\_eq}/Z_s}$. As a result, the other series inductor, $L_2(1-n)/n_2$, becomes sufficient small to be enforced either as an easy line within the layout or as a bonding wire [4].

C. Output Electrrical Phenomenon (Impedance) Matching

1. TWIN BAND NOTCH FILTER

Notch filter is employed to get rid of unwanted frequency, where having the notch, on that frequency the signal has been ejected. Association on-chip dual-band notch filter has been designed in Figure 5. This design is to be placed when the primary stage of proposed LNA and before the output. Here, to avoid the degradation in noise as a result of the loss of notch filter in LNA design, this stage is placed after the gain stage [2].

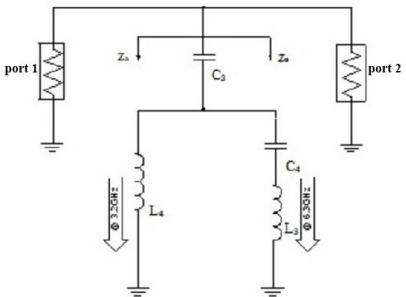

Fig. 5 Dual band notch filter

The impedance Z_A shown in the figure can be derived as,

$$Z_A = \frac{\omega^4 L_3 C_3 L_4 C_4 - \omega^2 (L_3 C_3 + L_3 C_4 + L_4 C_4) + 1}{j\omega C_3 [\,1 - \omega^2 (L_3 + L_4) C_4\,]} \quad (10)$$

The notch frequencies of the filter can be obtained by letting
the numerator equal null here,

$$\omega^4 L_3 C_3 L_4 C_4 - \omega^2 (L_3 C_3 + L_3 C_4 + L_4 C_4) + 1 = 0 \quad (11)$$

Which results in two transmission zeros ω_{Z1} and ω_{Z2}. They
satisfying,

$$\omega_{Z1}{}^2 * \omega_{Z2}{}^2 = \frac{1}{L_3\, C_3\, L_4\, C_4} \quad (12)$$

$$\omega_{Z1}{}^2 + \omega_{Z2}{}^2 = \frac{L_3 C_3 + L_3 C_4 + L_4 C_4}{L_3\, C_3\, L_4\, C_4} \quad (13)$$

Also from equation (10), the impedance Z_A contains a pole at,

$$\omega_{P1}{}^2 = \frac{1}{(L_3 + L_4) C_4} \quad (14)$$

The value of ω_{Z1}, ω_{Z2} and ω_{P1} were taken near about to 3.2, 6.3 and 4 GHz so the value of L_3, L_4, C_3 and C_4 can be obtained from the above equation for twin band notch filter in order to attenuate the interference.

2. CMOS INDUCTOR DESIGNING:

In this projected electronic equipment the conclusion of inductances L_3 and L_4 within the Notch Filter is by exploitation the active inductor. The active Inductor circuit uses thought of the Gyrator circuit. The advantage of the gyrator is that it may be enforced on an integrated circuit using transistors. The transistors act as transconductors and the changes to their bias points enable their trans-conductance to be tuned so that the inductance of active inductors may be varying. The inductance value of the active Inductor depends on the input/output voltage. Where's in passive inductor like planner and spiral inductor, it depends on the length of the planner/spiral structure. Therefore the space consumption is much more less in the active inductor as compare to the passive Inductor.

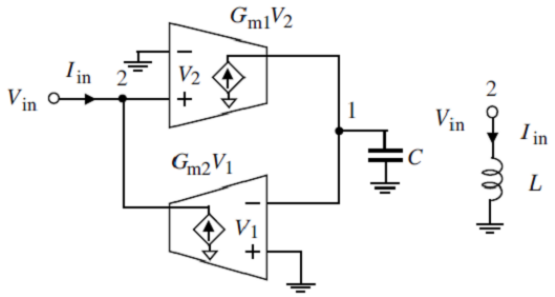

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Fig. 6 gyrator-c active inductor & its equivalent

A gyrator C abstract illustration is predicated on 2 trans-conductors is shown in Figure 6, it consists of 2 back to back connected trans-conductors and a capacitor is connected to 1 port of the gyrator, the network is termed the gyrator-C network. The Trans-conductor-1 provides a negative transconductance, g_{m1}, suggests that current through it flows into the trans-conductor once a positive voltage is applied at its input. The Trans-conductor-2 provides a positive trans-conductance; g_{m2} suggests that current flows out of the trans-conductor once at input a positive voltage is applied. Active Inductors may be divided into completely different sorts within which the primary is Lossless Single- Ended Gyrator-C Active Inductors which is loss less and have one finish as ground or supply voltage, and second is lossless Floating Gyrator-C active inductors which one end is loss less and used between 2 completely different nodes, and third one is lossy Single-Ended Gyrator-C active inductors that is once the gyrator-C networks are finite, than it'll not be lossless and it have one end as ground or supply voltage. Here during this application of LNA lossy single ended Gyrator C active Inductor has been used [2].

3. *Gyrator C Active Inductor(Lossy Single Ended):*

When trans-conductor's impedances either at input or at output of gyrator-C networks are finite, then the inductors won't be lossless. Also, on the particular frequency range, the gyrator-C networks are inductive. The gyrator-C network is as shown in Figure 7 where G_{o1} and G_{o2} denote the whole electrical conductance at nodes 1 and 2, respectively. Note G_{o1} is because to the finite output impedance of trans-conductor one and also the finite input impedance of trans-conductor 2.

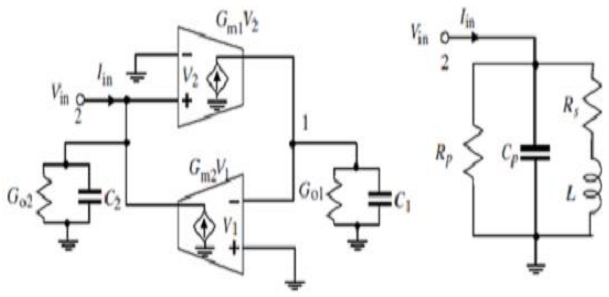

Fig. 7 Lossy single ended Gyrator-C Active Inductor

Equivalent RLC network shown in fig.9 can be represented by its parameter given by,

$$C_P = C_2\,,\ R_P = \frac{1}{G_{o2}}\,,\ L = \frac{C1}{G_{m1}\,G_{m2}}\,,\ R_S = \frac{G_{o1}}{G_{m1}\,G_{m2}} \quad (15)$$

The gyrator-C network acts as a lossy inductor with its parasitic parallel resistance Rp, parallel capacitance Cp, and series resistance Rs. Rp ought to be maximized whereas Rs ought to be reduced to low the ohmic loss. The finite input and output impedances of the trans-conductors of the gyrator-C network haven't any effect on the inductance of the active inductor. Rp and Cp are because of G_{o2} and C_2. G_{o1} and C_1 solely have an effect on Rs and L.

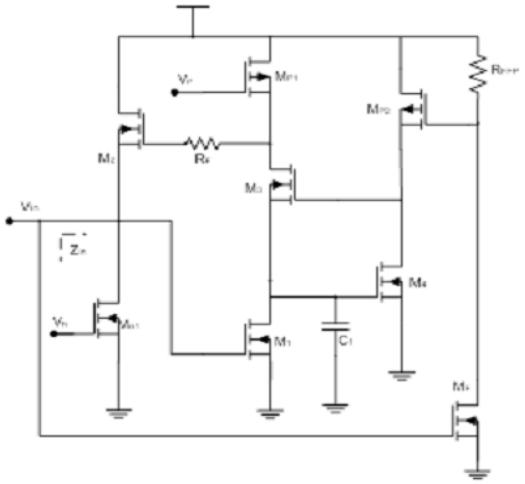

Fig. 8 Regulated Cascode F/B Resistive A.I. with Feed Forward Path

To enhance the value of Inductance likewise because the Quality issue, the cascode and controlled cascode topologies can be added to this lossy single ended gyrator C active Inductor. The regulated cascade with feedback resistor may be added to the gyrator C electronic equipment which may be wont to enhance Quality issue, Inductance and bandwidth of an Inductor [6]. To enhance the noise performance of the active inductor electronic equipment a feed-forward path (FFP) may be added to the bias input as shown in figure 8, the FFP comprising the common source transistor M_F and its resistive load R_F. This figure 8 provide the regulated cascode electronic equipment with feed forward path that improves the noise figure by increasing the bias current at M1 and together with that increase in the value of g_{m1} to reduce the input referred noise current [2].

IV. CONCLUSION

In this project we have understand the basic working concept of low noise amplifier, its output parameters, and characteristics which are important for various applications. A summarised method for analysing LNA circuit is discussed, with the underplaying assumptions and considered. On the whole, this project gives an over view of the working of low noise amplifier (LNA) for communication receiver circuit applications.

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