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REVIEW :- LOW POWER DOUBLE TAIL COMPARATOR BY CLOCK GATING

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Abstract:- The need for ultra low-power, area efficient, and high speed analog-to-digital converters is pushing toward the use of dynamic regenerative comparators to maximize speed and power efficiency. In the previous paper[19], an analysis on the delay of the dynamic comparators will be presented and analytical expressions are derived. From the analytical expressions, designers can obtain an intuition about the main contributors to the comparator delay and fully explore the tradeoffs in dynamic comparator design. Based on the presented analysis, a new dynamic comparator is proposed, where the circuit of a conventional double tail comparator is modified for low-power and fast operation even in small supply voltages. Without complicating the design and by adding few transistors, the positive feedback during the regeneration is strengthened, which results in remarkably reduced delay time. Post-layout simulation results in a 0.18-µm CMOS technology confirm the analysis results. It is shown that in the base paper proposed dynamic comparator both the power consumption and delay time are significantly reduced. In this paper , we are improving the performance of the system by use clock gating . After apply clock gating the delay and the power consumption will get reduce . Proposed system is giving the results for the 1.2 V Vdd . Channel length is using 130nm .

Index Terms—*Clock gating , Double-tail comparator, dynamic clocked comparator, high-speed analog-to-digital converters (ADCs), low-power analog design.*

I. INTRODUCTION

In electronics, a comparator is a device that compares two voltages or currents and outputs a digital signal indicating which is larger. It has two analog input terminals V+ and V- and one binary digital output Vo. The output is ideally

$$V0 = \begin{cases} 1, if\ V_+ > V_- \\ 0, if\ V_+ < V_- \end{cases} \quad \dots (1)$$

A comparator consists of a specialized high-gain differential amplifier. They are commonly used in devices that measure and digitize analog signals, such as analog-to-digital converters (ADCs), as well as relaxation oscillators.

A. Differential Voltage

The differential voltages must stay within the limits specified by the manufacturer. Early integrated comparators, like the LM111 family, and certain high-speed comparators like the LM119 family, require differential voltage ranges substantially lower than the power supply voltages (±15 V vs. 36 V).[1] Rail-to-rail comparators allow any differential voltages within the power supply range. When powered from a bipolar (dual rail) supply,

$$V_{S-} \le V_+ , V- \le V_{S+} \quad \dots (2)$$

or, when powered from a uni polar TTL/CMOS power supply:

$$0 \le V_+ , V- \le V_{cc} \quad \dots (3)$$

Specific rail-to-rail comparators with p-n-p input transistors, like the LM139 family, allow input potential to drop 0.3 volts below the negative supply rail, but do not allow it to rise above the positive rail.[2] Specific ultra-fast comparators, like the LMH7322, allow input signal to swing below the negative rail and above the positive rail, although by a narrow margin of only 0.2 V.[3] Differential input voltage (the voltage between two inputs) of a modern rail-to-rail comparator is usually limited only by the full swing of power supply.

B. Op - Amp Voltage Comparator

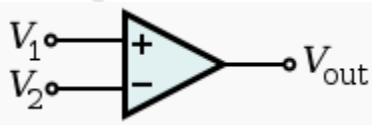

Fig 1 :- A simple op-amp comparator

An operational amplifier (op-amp) has a well balanced difference input and a very high gain. This parallels the characteristics of comparators and can be substituted in applications with low-performance requirements.[4]

In theory, a standard op-amp operating in open-loop configuration (without negative feedback) may be used as a low-performance comparator. When the non-inverting input (V+) is at a higher voltage than the inverting input (V-), the high gain of the op-amp causes the output to saturate at the highest positive voltage it can output. When the non-inverting input (V+) drops below the inverting input (V-), the output saturates at the most negative voltage it can output. The opamp's output voltage is limited by the supply voltage. An op-amp operating in a linear mode with negative feedback, using a balanced, split-voltage power supply, (powered by ± VS) has its transfer function typically written as: $V_{out} = A_0 (V_1 - V_2)$. However, this equation may not be applicable to a comparator circuit which is non-linear and operates open-loop (no negative feedback)

In practice, using an operational amplifier as a comparator presents several disadvantages as compared to using a dedicated comparator:[5]

- Op-amps are designed to operate in the linear mode with negative feedback. Hence, an op-amp typically has a lengthy recovery time from saturation. Almost all op-amps have an internal compensation capacitor which imposes slew rate limitations for high frequency signals. Consequently, an op-amp makes a sloppy comparator with propagation delays that can be as long as tens of microseconds.

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- Since op-amps do not have any internal hysteresis, an external hysteresis network is always necessary for slow moving input signals.
- The quiescent current specification of an op-amp is valid only when the feedback is active. Some op-amps show an increased quiescent current when the inputs are not equal.
- A comparator is designed to produce well limited output voltages that easily interface with digital logic. Compatibility with digital logic must be verified while using an op-amp as a comparator.
- Some multiple-section op-amps may exhibit extreme channel-channel interaction when used as comparators.
- Many op-amps have back to back diodes between their inputs. Op-amp inputs usually follow each other so this is fine. But comparator inputs are not usually the same. The diodes can cause unexpected current through inputs.

C. Working

A dedicated voltage comparator will generally be faster than a generalpurpose operational amplifier pressed into service as a comparator. A dedicated voltage comparator may also contain additional features such as an accurate, internal voltage reference, an adjustable hysteresis and a clock gated input.

A dedicated voltage comparator chip such as LM339 is designed to interface with a digital logic interface (to a TTL or a CMOS). The output is a binary state often used to interface real world signals to digital circuitry (see analog to digital converter). If there is a fixed voltage source from, for example, a DC adjustable device in the signal path, a comparator is just the equivalent of a cascade of amplifiers. When the voltages are nearly equal, the output voltage will not fall into one of the logic levels, thus analog signals will enter the digital domain with unpredictable results. To make this range as small as possible, the amplifier cascade is high gain. The circuit consists of mainly Bipolar transistors. For very high frequencies, the input impedance of the stages is low. This reduces the saturation of the slow, large P-N junction bipolar transistors that would otherwise lead to long recovery times. Fast small Schottky diodes, like those found in binary logic designs, improve the performance significantly though the performance still lags that of circuits with amplifiers using analog signals. Slew rate has no meaning for these devices. For applications in flash ADCs the distributed signal across eight ports matches the voltage and current gain after each amplifier, and resistors then behave as level-shifters.

The LM339 accomplishes this with an open collector output. When the inverting input is at a higher voltage than the non inverting input, the output of the comparator connects to the negative power supply. When the non inverting input is higher than the inverting input, the output is 'floating' (has a very high impedance to ground). The gain of op amp as comparator is given by this equation V(out)=V(in).

D. Conventional Dynamic Comparator

The schematic diagram of the conventional dynamic comparator widely used in A/D converters, with high input impedance, rail-to-rail output swing, and no static power consumption is shown in Fig. 2 [1], [17]. The operation of the comparator is as follows. During the reset phase when CLK = 0 and M_{tail} is off, reset transistors (M7–M8) pull both output nodes Out_n and Out_p to VDD to define a start condition and to have a valid logical level during reset. In the comparison phase, when CLK = VDD, transistors M7 and M8 are off, and M_{tail} is on.

Output voltages (Out_p, Out_n), which had been pre-charged to VDD, start to discharge with different discharging rates depending on the corresponding input voltage (INN/INP). Assuming the case where VINP > VINN, Outp discharges faster than Out_n, hence when Out_p (discharged by transistor M2 drain current), falls down to VDD–|Vthp| before Outn (discharged by transistor M1 drain current), the corresponding PMOS transistor (M5) will turn on initiating the latch regeneration caused by back-to-back inverters (M3, M5) and M4, M6). Thus, Outn pulls to VDD and Outp discharges to ground. If VINP < VINN, the circuits works vice versa. As shown in Fig. 2, the delay of this comparator is comprised of two time delays, t0 and t_{latch}.

The delay t0 represents the capacitive discharge of the load capacitance CL until the first p-channel transistor (M5/M6) turns on. In case, the voltage at node INP is bigger than INN (i.e., VINP > VINN), the drain current of transistor M2 (I2) causes faster discharge of Outp node compared to the Outn node, which is driven by M1 with smaller current.

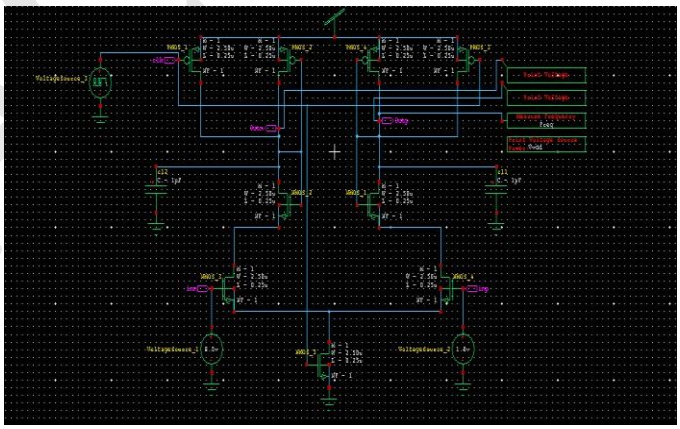

Fig 2 :- Conventional Dynamic Comparator

In principle, this structure has the advantages of high input impedance, rail-to-rail output swing, no static power consumption, and good robustness against noise and mismatch [1]. Due to the fact that parasitic capacitances of input transistors do not directly affect the switching speed of the output nodes, it is possible to design large input transistors to minimize the offset. The disadvantage, on the other hand, is the fact that due to several stacked transistors, a sufficiently high supply voltage is needed for a proper delay time.

The reason is that, at the beginning of the decision, only transistors M3 and M4 of the latch contribute to the positive feedback until the voltage level of one output node has dropped below a level small enough to turn on transistors M5 or M6 to start complete regeneration. At a low supply voltage, this voltage drop only contributes a small gate-source voltage for transistors M3 and M4, where the gate source voltage of M5 and M6

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is also small; thus, the delay time of the latch becomes large due to lower trans conductance.

Another important drawback of this structure is that there is only one current path, via tail transistor Mtail, which defines the current for both the differential amplifier and the latch (the cross-coupled inverters). While one would like a small tail current to keep the differential pair in weak inversion and obtain a long integration interval and a better Gm/I ratio, a large tail current would be desirable to enable fast regeneration in the latch [10]. Besides, as far as Mtail operates mostly in triode region, the tail current depends on input common-mode voltage, which is not favorable for regeneration.

E. Conventional Double-Tail Dynamic Comparator

A conventional double-tail comparator is shown in Fig. 3 [10]. This topology has less stacking and therefore can operate at lower supply voltages compared to the conventional dynamic comparator. The double tail enables both a large current in the latching stage and wider Mtail2, for fast latching independent of the input common-mode voltage (Vcm), and a small current in the input stage (small Mtail1), for low offset [10].

The operation of this comparator is as follows , During reset phase (CLK = 0, Mtail1, and Mtail2 are off), transistors M3-M4 pre-charge fn and fp nodes to VDD, which in turn causes transistors MR1 and MR2 to discharge the output nodes to ground. During decision-making phase (CLK = VDD, Mtail1 and Mtail2 turn on), M3-M4 turn off and voltages at nodes fn and fp start to drop with the rate defined by IMtail1/Cfn(p) and on top of this, an input-dependent differential voltage Vfn(p) will build up. The intermediate stage formed by MR1 and MR2 passes Vfn(p) to the cross coupled inverters and also provides a good shielding between input and output, resulting in reduced value of kickback noise [10].

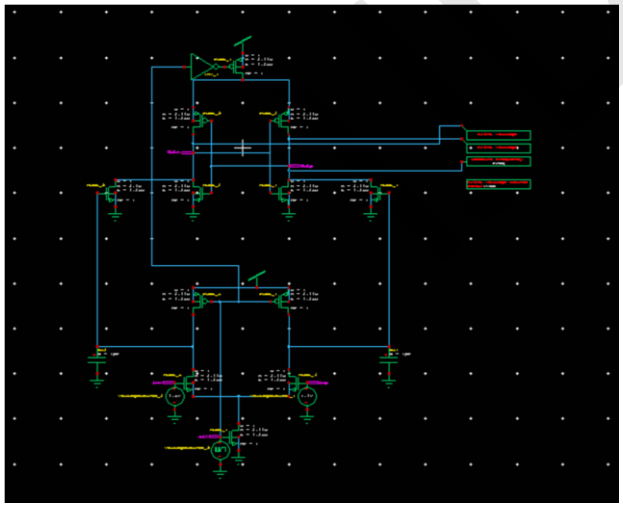

Fig 3 :- Conventional Double-Tail Dynamic Comparator

Similar to the conventional dynamic comparator, the delay of this comparator comprises two main parts, t0 and tlatch. The delay t0 represents the capacitive charging of the load capacitance CLout (at the latch stage output nodes, Outn and Outp) until the first n-channel transistor (M9/M10) turns on, after which the latch regeneration starts; thus t0 is obtained where IB1 is the drain current of the M9 (assuming VINP > VINN) and is approximately equal to the half of the tail current (Itail2). After the first n-channel transistor of the latch turns on (for instance, M9), the corresponding output (e.g., Outn) will be discharged to the ground, leading front p-channel transistor (e.g., M8) to turn on, charging another output (Outp) to the supply voltage (VDD).

F. Double-Tail Dynamic Comparator

Due to the better performance of double-tail architecture in low-voltage applications, the proposed comparator is designed based on the doubletail structure. The main idea of the proposed comparator is to increase Vfn/fp in order to increase the latch regeneration speed. For this purpose, two control transistors (Mc1 and Mc2) have been added to the first stage in parallel to M3/M4 transistors but in a cross-coupled.

- *Operation of Comparator*

During reset phase (CLK = 0, Mtail1 and Mtail2 are off, avoiding static power), M3 and M4 pulls both fn and fp nodes to VDD, hence transistor Mc1 and Mc2 are cut off. Intermediate stage transistors, MR1 and MR2, reset both latch outputs to ground.

During decision-making phase (CLK = VDD, Mtail1, and Mtail2 are on), transistors M3 and M4 turn off. Furthermore, at the beginning of this phase, the control transistors are still off (since fn and fp are about VDD). Thus, fn and fp start to drop with different rates according to the input voltages. Suppose VINP > VINN, thus fn drops faster than fp, (since M2 provides more current than M1). As long as fn continues falling, the corresponding pMOS control transistor (Mc1 in this case) starts to turn on, pulling fp node back to the VDD so another control transistor (Mc2) remains off, allowing fn to be discharged completely. In other words, unlike conventional double-tail dynamic comparator, in which Vfn/fp is just a function of input transistor trans conductance and input voltage difference (9), in the structure as soon as the comparator detects that for instance node fn discharges faster, a PMOS transistor (Mc1) turns on, pulling the other node fp back to the VDD.

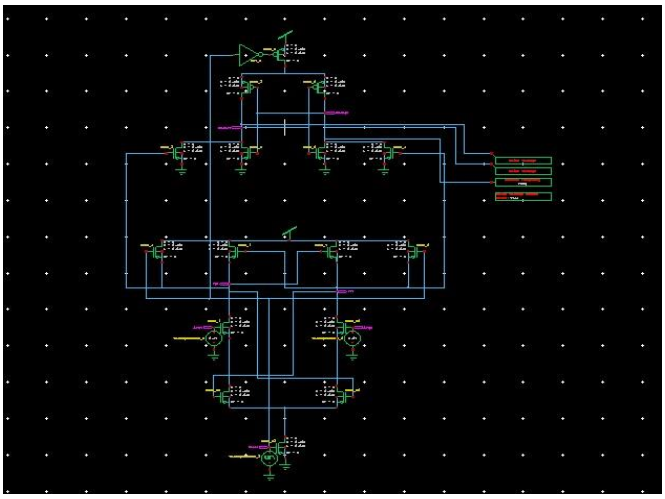

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Fig 4 :- Double Tail Comparator

Therefore by the time passing, the difference between fn and fp (Vfn/fp) increases in an exponential manner, leading to the reduction of latch regeneration time . Despite the effectiveness of the proposed idea, one of the points which should be considered is that in this circuit, when one of the control transistors (e.g., Mc1) turns on, a current from VDD is drawn to the ground via input and tail transistor (e.g., Mc1, M1, and Mtail1), resulting in static power consumption. To overcome this issue, two NMOS switches are used below the input transistors Msw1 and Msw2.

At the beginning of the decision making phase, due to the fact that both fn and fp nodes have been pre-charged to VDD (during the reset phase), both switches are closed and fn and fp start to drop with different discharging rates. As soon as the comparator detects that one of the fn/fp nodes is discharging faster, control transistors will act in a way to increase their voltage difference. Suppose that fp is pulling up to the VDD and fn should be discharged completely, hence the switch in the charging path of fp will be opened (in order to prevent any current drawn from VDD) but the other switch connected to fn will be closed to allow the complete discharge of fn node. In other words, the operation of the control transistors with the switches emulates the operation of the latch.

II. PROBLEM STATEMENT

We can further improve the performance of the double tail comparator in terms of delay and power . In the base paper proposed circuit , the power is consuming in entire circuit too much . We can further reduce the power consumption from the base paper circuit power . The need for ultra low-power, area efficient, and high speed analog-to-digital converters is pushing toward the use of dynamic regenerative comparators to maximize speed and power efficiency. In the base paper, an analysis on the delay of the dynamic comparators will be presented and analytical expressions are derived. From the analytical expressions, designers can obtain an intuition about the main contributors to the comparator delay and fully explore the tradeoffs in dynamic comparator design. Based on the presented analysis, a new dynamic comparator is proposed in the base paper , where the circuit of a conventional double tail comparator is modified for low-power and fast operation even in small supply voltages.

III. PROPOSED METHODOLOGY

Clock gating is a popular technique used in many synchronous circuits for reducing dynamic power dissipation. Clock gating saves power by adding more logic to a circuit to prune the clock tree. Pruning the clock disables portions of the circuitry so that the flip-flops in them do not have to switch states. Switching states consumes power. When not being switched, the switching power consumption goes to zero, and only leakage currents are incurred.

Clock gating works by taking the enable conditions attached to registers, and uses them to gate the clocks. Therefore it is imperative that a design must contain these enable conditions in order to use and benefit from clock gating. This clock gating process can also save significant die area as well as power, since it removes large numbers of muxes and replaces them with clock gating logic. This clock gating logic is generally in the form of "Integrated clock gating" (ICG) cells. However, note that the clock gating logic will change the clock tree structure, since the clock gating logic will sit in the clock tree. Clock gating logic can be added into a design in a variety of ways:

- Coded into the RTL code as enable conditions that can be automatically translated into clock gating logic by synthesis tools (fine grain clock gating).
- Inserted into the design manually by the RTL designers (typically as module level clock gating) by instantiating library specific ICG (Integrated Clock Gating) cells to gate the clocks of specific modules or registers.
- Semi-automatically inserted into the RTL by automated clock gating tools. These tools either insert ICG cells into the RTL, or add enable conditions into the RTL code. These typically also offer sequential clock gating optimizations.

Any RTL modifications to improve clock gating will result in functional changes to the design (since the registers will now hold different values) which need to be verified.

Sequential clock gating is the process of extracting/propagating the enable conditions to the upstream/downstream sequential elements, so that additional registers can be clock gated.

Although asynchronous circuits by definition do not have a "clock", the term perfect clock gating is used to illustrate how various clock gating techniques are simply approximations of the data-dependent behavior exhibited by asynchronous circuitry. As the granularity on which you gate the clock of a synchronous circuit approaches zero, the power consumption of that circuit approaches that of an asynchronous circuit: the circuit only generates logic transitions when it is actively computing.

Chip families such as OMAP 3, with a cell phone heritage, support several forms of clock gating. At one end is the manual gating of clocks by software, where a driver enables or disables the various clocks used by a given idle controller. On the other end is automatic clock gating, where the hardware can be told to detect whether there's any work to do, and turn off a given clock if it is not needed. These forms interact with each other and may be part of the same enable tree. For example, an internal bridge or bus might use automatic gating so that it is gated off until the CPU or a DMA engine needs to use it, while several of the peripherals on that bus might be permanently gated off if they are unused on that board.

Clock tree consume more than 50 % of dynamic power. The components of this power are:

- Power consumed by combinatorial logic whose values are changing on each clock edge .
- Power consumed by flip-flops
- The power consumed by the clock buffer tree in the design.

It is good design idea to turn off the clock when it is not needed. Automatic clock gating is supported by modern EDA tools. They identify the circuits where clock gating can be inserted.

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IV. CONCLUSION

In this thesis, we presented a comprehensive delay analysis for clocked gating dynamic comparators and expressions were derived. Two common structures of conventional dynamic comparator and conventional double-tail dynamic comparators were analyzed. Also, based on theoretical analyses, a new dynamic comparator with lowvoltage low-power capability was proposed in order to improve the performance of the comparator. Post-layout simulation results in 0.13μm CMOS technology confirmed that the delay and energy per conversion of the proposed comparator is reduced to a great extent in comparison with the conventional dynamic comparator and double-tail comparator.

In the future , we can further improve the performance of the system by use GDI and modified GDI technique . GDI is also capable for reduce the power consumption of the circuit . GDI can be apply in clock gating circuit so that further power can be reduce .

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