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Design & Implementation of AHB Interface for SOC Application

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***Abstract*— In The AMBA™ on-chip interconnect system is an established open specification that details a strategy on the interconnection and management of functional blocks that makes up a System-on-Chip (SoC).**

In this work, the design and implementation of an AMBA based AHB Master and AHB Slave with Memory controller interface is proposed. It is majorly categorized in two dedicated feature i.e. decision (AHB MASTER) and response (AHB SLAVE).

Moreover AHB master enables transfer types i.e. burst mode and AHB Master-to-AHB slave supports incrementing and wrapping addressing modes and completes data transfer which the data width of read and write is different by asymmetric asynchronous FIFO .A bridge between AHB Master and AHB slave with application of memory controller will been shown and there digital efficiency in terms of area and speed will be discussed. Control structure will be designed with finite state machine. The IP of AHB Master and AHB Slave will been implemented in Xilinx Spartan-3 3s50pq208-5.

***Keywords* — AMBA, AHB Master, AHB Slave, SOC.**