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VHDL Implementation of High Speed AXI2.0 Protocol with DDR3 Controller

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Abstract –**This paper proposes the implementation of AXI 2.0 protocol which removes the limitation of communication architecture, which would otherwise reduce the speed of data transfer in System-on-Chip (SoC). We have also implemented DDR3 controller which was then interface with AXI 2.0 protocol. Proposed protocol was synthesized on Xilinx 13.1 and simulated using Modelsim 6.5e.**

Keywords – **AXI 2.0, DDR3, Modelsim, SoC, Xilinx.**