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# An Efficient AXI Read and Write Channel for Memory Interface in System-on-Chip

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*Abstract* –**System-on-a-Chip (SoC) design has become more and more complexly. Because difference functions components or IPs (Intellectual Property) will be integrated within a chip. The challenge of integration is "how to verify on-chip communication properties". Although traditional simulation-based on-chip bus protocol checking bus signals to obey bus transaction behaviour or not, however, they are still lack of a chip-level dynamic verification to assist hardware debugging. This paper proposes an efficient AXI read and write channel for memory interface in SOC.**

*Keywords* –**Intellectual Property, SoC, AXI.**