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# CPLD Implementation of Digital PLL for Maintaining Speed of DC Motor

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***Abstract*— This paper explains a method for implementation of a digital PLL for speed control of a DC motor at varying load conditions using Programmable Logic Device (CPLD) device. It is more compact, power efficient, EEPROM based, cheaper and provides high speed capabilities as compared to software based PLL controllers. The proposed method is based on implementation of digital PLL controller for speed control of DC motor. The PLL controller is designed using QUARTUS and Simulink to generate a set of parameters associated with the desired controller. The architecture was implemented on hardware to give flexibility and compatibility with the Simulink design of a controller. The controller parameters are then included in VHDL that implements the PLL controller for speed control on to CPLD. QUARTUS program is used to design PLL controller to calculate and plot the time response of the control system as per speed variation.PWM technique is used to trigger the gate junction of the MOSFET which in turn is utilized to vary the input voltage of DC motor ,thus controlling the speed.**

***Keywords*— CPLD, DPLL, DC motor, Speed controller, PWM generator, Phase frequency detector, QUTRAUS.**

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