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A BIST Architecture based UART Transmitter for Digital Verification

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Abstract –**External devices such as modems and other computers need to communicate serially. In order to provide this communication, a universal asynchronous receiver transmitter (UART) can provide an asynchronous serial data communication with I/O outputs devices such as keyboard, mouse or keypad. Built-In-Self-Test (BIST) is the most common design technique that allows self-testability to avoid the product failures. A Universal Asynchronous Receiver Transmitter (UART), mostly used for short distance, low speed, low cost data exchange between processor and peripherals. UART allows full duplex serial communication link, also used in control system and data communication. There is a need for realizing the UART function in a single chip. This paper presents a VHDL implementation of UART design with embedded BIST technique over FPGA.**

Keywords –**BIST, FPGA, UART, VHDL.**