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Comparison of Various n-T SRAM Cell for Improvement of Power, Speed and SNM

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Abstract - **Low Power VLSI Circuit has greater demand in present world, Power consumption is very less in CMOS circuit design, so we built SRAM using CMOS which consume less power and have less read and write time. This trend decrease device size and increase chip density, by fabricating million of transistor over a single chip. The read and write operation depends on charging and discharging of bit line and bit line bar. To enhance the performance of the SRAM cell static noise margin (SNM) has to be improved. In this paper we have different structure of SRAM cell, and measure the different parameters like average power delay PDP and SNM, by using Cadence virtuoso simulator at 180nm CMOS technology, simulator shows that at least 20%-45% write power saving, with higher stability, with no degradation of performance with increase of additional 15.25% silicon area.**

Keywords - **SRAM cell, Read/write operation, Low Power, SNM, Bit line.**