IJDACR
ISSN: 2319-4863

IJDACR
International Journal Of Digital Application & Contemporary Research

International Journal of Digital Application & Contemporary Research
Website: www.ijdacr.com (Volume 4, Issue 11, June 2016)

VHDL Implementation of BIST Enabled UART

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Abstract – **This paper introduces a novel approach of Linear Feedback Shift Resister (LFSR) for Built-in-self-test (BIST) along with 8 bit UART, to overcome testability and data integrity. The complete design is implemented in VHDL and simulated throughout in Modelsim, synthesis is carried out in Xilinx 14.1. The IP core is implemented on FPGA device 3s500efg320-4. The results indicate that this model eliminates the need of higher end, expensive testers and thereby it can reduce the development time and cost.**

Keywords – **BIST, FPGA, LFSR, Modelsim, UART, VHDL, Xilinx.**