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RTL Implementation of AXI Interface for Memory Controller

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Abstract –**This paper proposes an implementation of AXI 2.0 protocol which removes the limitation of communication architecture, which would otherwise reduce the speed of data transfer in System on chip. We have also implemented DDR3 controller which was then interface with AXI 2.0 protocol. Proposed protocol was synthesized on Xilinx 13.1 and simulated using Modelsim 6.5e.**

Keywords – **AXI, DDR3, Modelsim, Xilinx.**