IJDACR
ISSN: 2319-4863

IJDACR
International Journal Of Digital Application & Contemporary Research

International Journal of Digital Application & Contemporary research
Website: www.ijdacr.com (Volume 1, Issue 7, February 2013)

Programmable FSM based MBIST Architecture

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Abstract - **SOCs comprise of wide range of memory modules so it is not possible to test all the memory modules with the help of a single algorithm. Each memory type may require a distinct test algorithm. Implementing an MBIST to test each memory module would result in a high production cost; hence it makes more sense to use a programmable MBIST for entire chip instead of using it for individual memory modules. In this research, FSM based programmable memory BIST architecture is proposed which can select March algorithms to test the memory. Use of various March algorithms provides flexibility in applying different test patterns. Experimental results indicate that the proposed architecture achieves improved test flexibility, lower testing cost, high frequency and the area overhead is effectively reduced for some algorithms.**

Keywords – **SOC, MBIST, FSM, March Algorithms.**