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A Review on Bus Interfaces of AMBA

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Abstract – **Today's system-on--chip (SOC) is designed with reusable intellectual property cores to meet short time to market requirements. Embedded systems design focuses on low Power dissipation and system-on-chip. A reliable on-chip communication standard is a must in any SOC. This paper gives an informative review about the bus interfaces of Advanced Microcontroller Bus Architecture (AMBA).**

Keywords – **Bus Interface, AMBA.**

I. INTRODUCTION

The Advanced Microcontroller Bus Architecture (AMBA) specification defines an on chip communications standard for designing high-performance embedded microcontrollers. Three distinct buses are defined within the AMBA specification.

- Advanced High-performance Bus (AHB)
- Advanced System Bus (ASB)
- Advanced Peripheral Bus (APB)

A test methodology is included with the AMBA specification which provides an infrastructure for modular macrocell test and diagnostic access.

II. ADVANCED HIGH-PERFORMANCE BUS (AHB)

AHB is a new generation of AMBA bus which is intended to address the requirements of high-performance synthesizable designs. It is a high performance system bus that supports multiple bus masters and provides high bandwidth operation. AMBA AHB implements the features required for high performance, high clock frequency systems including:

- Burst transfers
- Split transactions
- Single-cycle bus master handover
- Single-clock edge operation
- Non-tristate implementation
- Wider data bus configurations (64/128 bits)

Bridging between this higher level of bus and the current ASB/APB can be done efficiently to ensure that any existing designs can be easily integrated. An AMBA AHB design may contain one or more bus masters, typically a system would contain at least the processor and test interface. However, it would also be common for a Direct Memory Access (DMA) or Digital Signal Processor (DSP) to be included as bus masters. The external memory interface, APB Bridge and any internal memory are the most common AHB slaves. Any other peripheral in the system could also be included as an AHB slave. However, low-bandwidth peripherals typically reside on APB.

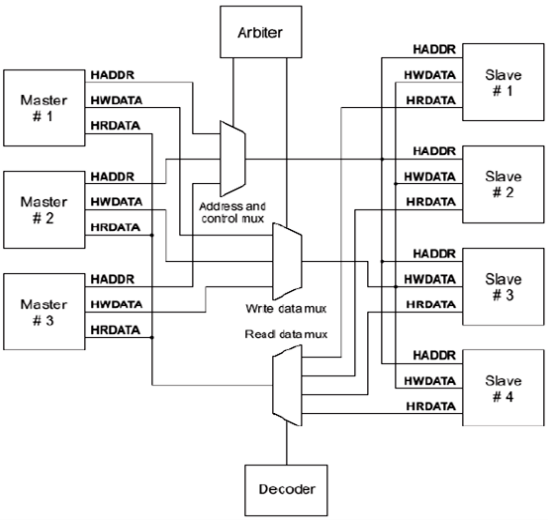

Figure 1: AMBA AHB Block diagram

A typical AMBA AHB system design contains the following components:

1. **AHB Master:** A bus master is able to initiate read and write operations by providing an address and control information. Only one bus master is allowed to actively use the bus at any one time.

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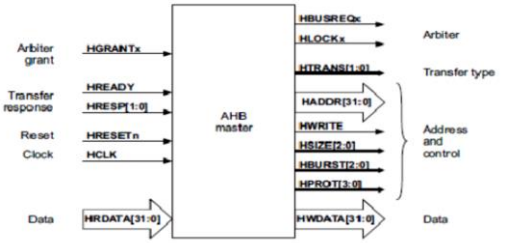

Figure 2: AHB bus master Interface

2. **AHB Slave:** A bus slave responds to a read or write operation within a given address-space range. The bus slave signals back to the active master the success, failure or waiting of the data transfer.

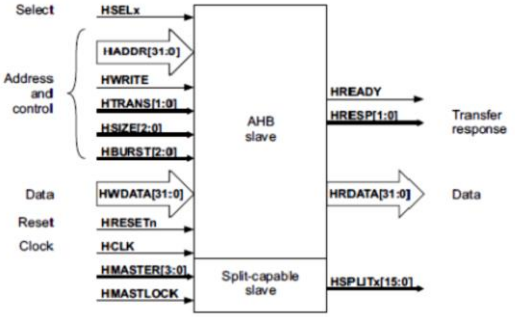

Figure 3: AHB bus slave interface

3. **AHB Arbiter:** The bus arbiter ensures that only one bus master at a time is allowed to initiate data transfers. Even though the arbitration protocol is fixed, any arbitration algorithm, such as highest priority or fair access can be implemented depending on the application requirements. An AHB would include only one arbiter, although this would be trivial in single bus master.

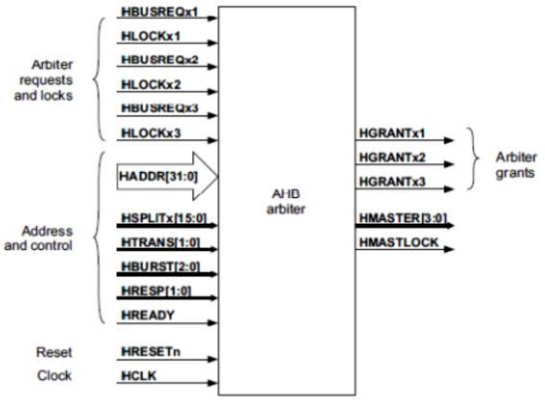

Figure 4: AHB arbiter interface

4. **AHB Decoder:** The AHB decoder is used to decode the address of each transfer and provide a select signal for the slave that is involved in the transfer. A single centralized decoder is required in all AHB implementations.

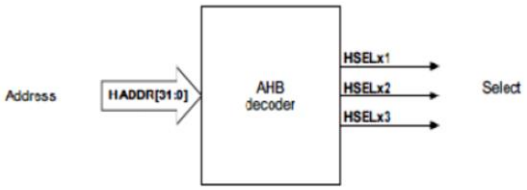

Figure 5: AHB decoder interface

III. AMBA ADVANCED PERIPHERAL BUS (APB)

The APB is part of the AMBA hierarchy of buses and is optimized for minimal power consumption and reduced interface complexity. The AMBA APB appears as a local secondary bus that is encapsulated as a single AHB or ASB slave device. APB provides a low-power extension to the system bus which builds on AHB or ASB signals directly. The APB bridge appears as a slave module which handles the bus handshake and control signal retiming on behalf of the local peripheral bus. By defining the APB interface from the starting point of the system bus, the benefits of the system diagnostics and test methodology can be exploited. The AMBA APB should be used to interface to any peripherals which are low band width and do not require the high performance of a pipelined bus interface. The latest revision of the APB is specified so that all signal transitions are only related to the rising edge of the clock. This improvement ensures the APB peripherals can be integrated easily into any design flow, with the following advantages:

- High-frequency operation easier to achieve.
- Performance is independent of the mark-space ratio of the clock.
- Static timing analysis is simplified by the use of a single clock edge.
- No special considerations are required for automatic test insertion.
- Easy integration with cycle-based simulators.
- Many Application Specific Integrated Circuit (ASIC) libraries have a better Selection of rising edge registers.

These changes to the APB also make it simpler to interface it to the new AHB. An AMBA APB implementation typically contains a single APB bridge which is required to convert AHB or ASB transfers into a suitable format for the slave devices on the APB.

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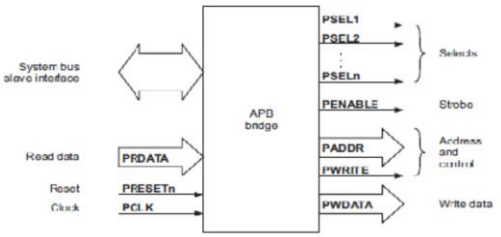

Figure 6: APB Bridge interfacing diagram

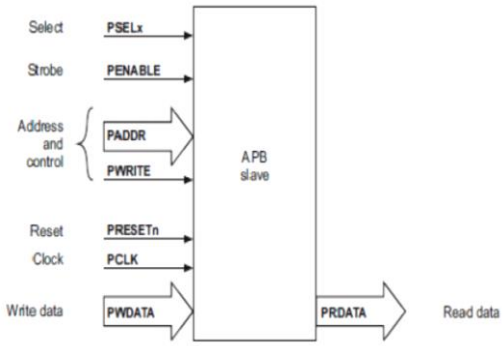

Figure 7: APB slave interfacing diagram

The bridge provides latching of all address, data and control signals, as well as providing a second level of decoding to generate slave select signals for the APB peripherals. All other modules on the APB are APB slaves. The APB slaves have the following interface specification:

- Address and control valid throughout the access (un-pipelined)
- Timing can be provided by decode with strobe timing (un-clocked interface)
- Zero-power interface during non-peripheral bus activity (peripheral bus is static when not in use)
- Write data valid for the whole access (allowing glitch-free transparent latch implementations).

IV. AMBA SPECIFICATION

The following points should be considered when reading the AMBA specification:

- Technology independence
- Electrical characteristics
- Timing specification

Technology independence: AMBA is a technology-independent on-chip protocol. The specification only details the bus protocol at the clock cycle level. *Electrical characteristics:* No information regarding the electrical characteristics is supplied within the AMBA specification as this will be entirely dependent on the manufacturing process technology that is selected for the design.
Timing specification: The AMBA protocol defines the behaviour of various signals at the cycle level. The exact timing requirements will depend on the process technology used and the frequency of operation.

AMBA Signal Names

- All AMBA signals are named such that the first letter of the name indicates which bus the signal is associated with.
- A lower case n in the signal name indicates that the signal is active LOW, otherwise signal names are always all upper case.
- Test signals have a prefix T regardless of the bus type AHB signal prefixes-H indicates an AHB signal. For example, HREADY is the signal used to indicate that the data portion of an AHB transfer can complete. It is active HIGH.
- APB signal prefixes-P indicates an APB signal. For example, PCLK is the main clock used by the APB.

Choice of Bus

Before deciding on which bus or buses should use in system should consider the following:

- Choice of system bus
- System bus and peripheral bus
- When to use AMBA AHB/ASB or APB

Choice of system bus-Both AMBA AHB and ASB are available for use as the main system bus. Typically the choice of system bus will depend on the interface provided by the system modules required The AHB is recommended for all new designs, not only because it provides a higher bandwidth solution, but also because the single-clock-edge protocol results in a smoother integration with design automation tools used during a typical ASIC development. System bus and peripheral bus-Building all peripherals as fully functional AHB or ASB modules is feasible but may not always be desirable:

- In designs with a large number of peripheral macrocells the increased bus loading may increase power dissipation and sacrifice performance.
- Where timing analysis is required, the slowest element on the bus will limit the maximum performance.
- Many simple peripheral macrocells need latched addresses and control signals as

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opposed to the high-bandwidth macrocells which benefit from pipelined signalling.

- Many peripheral functions simply require a selection strobe which conveys macrocell selection and read/write bus operation, without the requirement to broadcast the high-frequency clock signal to every peripheral.

When to use AMBA AHB/ASB or APB- A full AHB or ASB interface is used for:

- Bus masters
- On-chip memory blocks
- External memory interfaces
- High-bandwidth peripherals with FIFO interfaces
- DMA slave peripherals

A simple APB interface is recommended for:

- Simple register-mapped slave devices.
- Very low power interfaces where clocks cannot be globally routed
- Grouping narrow-bus peripherals to avoid loading the system bus.

V. CONCLUSION

Carrying out literature review is very significant in any research project. It clearly establishes the need of the work and the background development. It generates related queries regarding improvements in the study already done and allows unsolved problems to emerge and thus clearly define all boundaries regarding the development of the research work. This paper reviews the bus architectures of AMBA 2.0.

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