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Multiplier-Accumulator (MAC) Unit

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Abstract: **The MAC unit is a unit that is mostly demanded in DSP applications. MAC unit performs both multiply and addition functions. It operates in two stages. Firstly it computes the product of given numbers and forward the result for the second stage operation i.e. addition/accumulate. If both the computing is executed in a single rounding then it is said to be fused multiply-add/accumulate (MAC) unit. There has been a lot of research performed on MAC implementation. This paper provides a comparative study and analysis of the research and investigations held till now.**

Keywords: **CMOS, DTMAC, DSP, ECSM, FPGA, MAC, VLSI.**

I. INTRODUCTION

The Multiplier-accumulator (MAC) unit supports large number of digital signal processing (DSP) applications. It also furnishes signal processing ability to the microcontroller for various applications such as servo/audio control etc. MAC, being an execution unit in the processor implements a 3-stage pipelined arithmetic architecture which optimizes 16×16 multipliers. This design supports both 16-bit and 32-bit operands. It also supports signed/unsigned integers plus signed, fixed-point fractional input operands [2].

The MAC unit supports mainly three functions:

- Signed and unsigned integer multiplies
- Multiply-accumulate operations supporting signed, unsigned, and signed fractional operands
- Miscellaneous register operations

An accumulator adder and multiplier together form a MAC unit. Usually Carry-select/Carry-save adders are mostly implemented due to the DSP application requirement of fast speed [1]. The memory fetches the inputs from its location to multiplier for further multiply-accumulate operations. The generated result of MAC unit is stored at a relevant memory location. The situation demands that this complete process should be carried out into a single clock cycle [1].

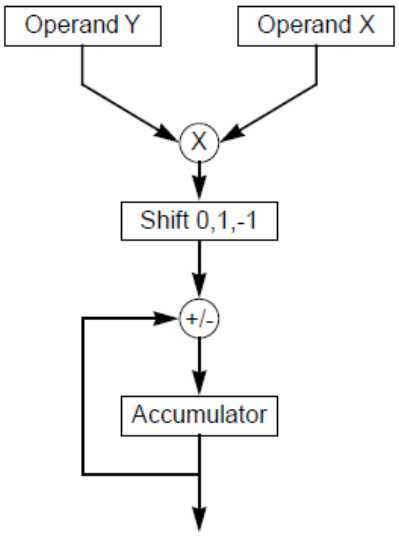

Figure 1: Block diagram of MAC unit

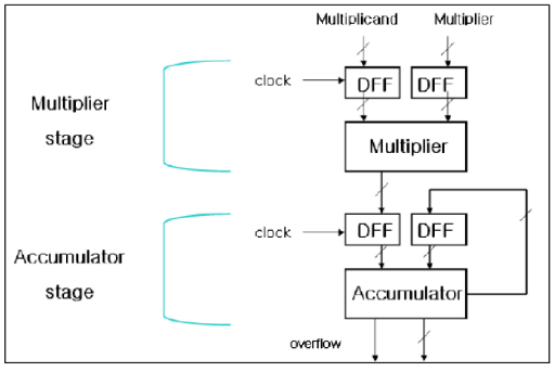

Figure 2: Architecture of MAC unit [1]

The idea behind developing MAC unit is taken from basic multiplier. We can say MAC unit is a further version of basic multiplier unit which is used by almost all microprocessors. It supports large number of digital signal processing (DSP) applications within limited number of cycles as per application demand. Like some of the filters can adjust a delay during execution but the algorithms such as orthogonal transforms etc. demands accurate speed execution/measurement which

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sometimes can be beyond the processor capability [2].

II. LITERATURE REVIEW

Wide range of applications such as graphics designing, DSP applications, multimedia, image processing etc. use multiply-accumulate (MAC) functions for its efficient arithmetic operations. MAC arithmetic operations can be fused multiply-addition operations i.e. multiplication followed by addition/subtraction. In reference paper [3], low-precision FP multiply-addition fused units are proposed which depends upon FPGA characteristics so that the MAC (multiply-accumulate) can support the DSPs. In order to use DSPs efficiently and to achieve high performance thereby saving the system cost, aligning and shifting is done prior to the multiply-add stage. This includes right shifting of addend and multiplicands. This proposed method suits well for low-precision formats like half precision where only one digital signal processing block is used for multiplication. This method gives high performance and 25% cost effectiveness when compared with other approaches [3].

In reference paper [2], a high speed 2-cycle MAC architecture is proposed which also energy efficient. MAC architecture includes saturation circuitry and guard bits and it also supports 2's complement numbers. 1st pipeline MAC stage is comprised of reduction tree and partial-product circuit only whereas the 2nd pipeline MAC stage is comprised of all other extra functions. The observations state that this new architecture is 31% faster in computation and decrease energy/operation by 32%. This new architecture is being used in order to develop a versatile MAC block i.e. double-throughput MAC (DTMAC) that supports various modes of operations i.e. 3 for multiply-accumulate mode and 3 for multiply operations.

Wireless sensor networks have a lot many risks when it comes to energy efficiency and security concerns. This paper [4] proposed an energy efficient approach for securing the network against the attacks that can lessen network's lifetime are also known as power exhausting attacks like Denial-of-Sleep attack.

The reference paper [5] proposes techniques for logarithmic (LNS) addition/subtraction and states its effect on digital filter implemented using VLSI technology. For LNS calculations/arithmetic operations, partitioning of Look-up-tables (LUT) is used which divides the circuit into small parts which can be accessed easily thereby decreasing power dissipation and complexity of the system. The overview of proposed method is depicted in Fig. 3.

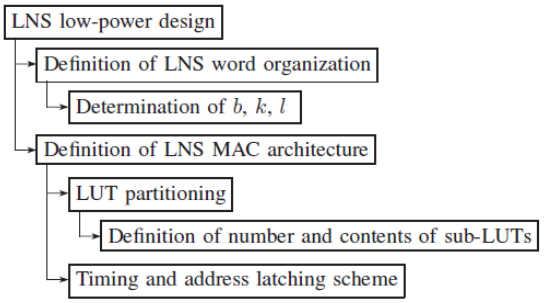

Figure 3: Overview of Low-power LNS design

Network's complexity can be minimized by exploiting LNS base and LNS word parameters. Furthermore, after researching low-power implementation techniques on LNS-MAC units, it is expected that the future work can be extended to interpolators based circuitry. The performance of FIR filters employing 1 or more than one (up to 4) MAC units is evaluated on the basis of power dissipation and complexity parameters. The results reveal that the proposed technique makes power savings possible with no performance degradation when compared with other equivalent circuits [5].

In reference paper [6], a pipelined architecture is described for elliptic curve scalar multiplication (ECSM) over GF(2^m). This architecture makes use of multiplier-accumulator (MAC) of finite field of order 2^m. Proposed architecture is designed on the basis of Karatsuba-ofman algorithm in order to reduce the area. On the other hand, data paths are designed on the basis of Montgomery ladder algorithm so as to obtain shortest data-path execution. The goal of this article is to speed-up the ECSM thereby achieving area reduction. The architecture is comprised of mainly two blocks:

1) Non-pipelined FF Squarer and
2) Pipelined bit-parallel FF MAC

Thorough analysis of pipeline registers helps to determine the optimal no. of pipeline stages which states that the proposed method is far better than the existing methods in terms of area and speed [6].

Various practical applications such as image restoring and signal recovery obtained by inclusive sensing utilize sparse signal recovery mechanism. Reference paper [7] proposes two VLSI models that implements approximate message passing (AMP) algorithm (depicted in Fig. 4) for sparse signal recovery. The two architectures are as follows:

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1) *AMP-M:* This architecture uses MAC units and resolves unstructured/arbitrary/random matrices recovery problems.
2) *AMP-T:* This architecture is designed especially for the recovery issues occurred due to measurement matrices that exploits fast transform algorithms.

Approximate Message Passing (AMP)Algorithm

initialize $\mathbf{r}^0 = \mathbf{z}$ and $\mathbf{x}^0 = \mathbf{0}_{N\times 1}$

for $i = 1, \ldots, I_{\max}$ **do**

$\theta \leftarrow \lambda(1/\sqrt{M})\|\mathbf{r}^{i-1}\|_2$

$\mathbf{x}^i \leftarrow \eta_\theta(\mathbf{x}^{i-1} + \mathbf{D}^T\mathbf{r}^{i-1})$

$b \leftarrow (1/M)\|\mathbf{x}^i\|_0$

$\mathbf{r}^i \leftarrow \mathbf{z} - \mathbf{D}\mathbf{x}^i + b\mathbf{r}^{i-1}$

end for

return $\mathbf{x}^{I_{\max}}$

Figure 4: Approximate Message Passing Algorithm

To evaluate the performance of both architectures, the architectures are implemented on 65nm CMOS technology using VLSI and FPGA platforms. The results demonstrate that AMP-T architecture is better than AMP-M architecture. Although AMP-M provides flexibility advantage but AMP-T has better performance in terms of power consumption, area and throughput [7].

The analysis and the statistic data over last thirty years prove that there is a huge decrease in the energy efficiency rate. The reason behind this is supposed to be an "asymptotic wall" with the dataset. For this reason an energy model is proposed in this paper [8] which considers scale and specifications of asynchronous systems. The system is simulated on 0.6µm and 65nm process with the power performance of 1.58pJ per unit operation. However it does not meet the target of 10J per unit operation [8].

In reference paper [9], a new MAC architecture is proposed with introducing a carry-save adder which improves the performance. This new architecture uses Booth's algorithm which is based on 1's complement radix-2 basis. The carry-save adder diverts the carry towards LSB of partial product and in order to decrease the final bits of the adder, CSA generates LSBs. This helps in implementing pipeline approach which in turn improves the performance. In this proposed scheme the main motive is to remove the independent accumulate stage which creates a huge delay and merge it with partial product's compression stage. This enhances system's performance almost twice [9].

There is a huge research done on the implementation of MAC unit in different operating blocks such as filters, adders, multipliers, squarers etc. The proposed design and idea behind its implementation given in brief as below:

Designing of FIR filter using Carry Look Ahead adder and Booth multiplier helps in making FIR filter operate faster. Booth multiplier works on the principle of "state machine". Proposed architecture can operate for 'n' number of bits but here n is taken to 16 (n=16). Proposed MAC architecture is very high speed architecture which makes FIR filter operates faster [10].

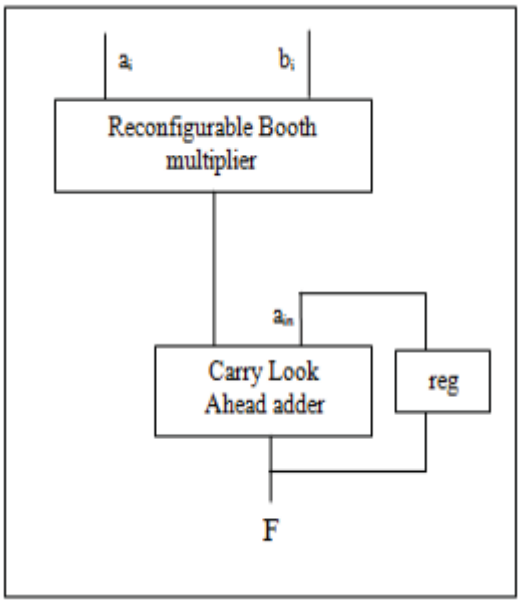

Figure 5: Proposed MAC unit [10]

In reference paper [11], MAC units are implemented into two designs i.e. regular redundant carry-save array type and hybrid double carry-save type. The regular design needs more area as compared to hybrid design and hybrid design achieves peak throughput among other carry-free and carry-propagate designs. Whenever a high performance is desired, hybrid design is preferred as it is also scalable [11].

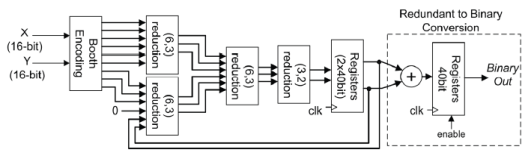

Figure 6: Proposed MAC architecture [11]

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A fused MAC is designed in paper [12] which has low clock frequency and high throughput. The architecture contains logic depth in a very less quantity and also it is free from carry propagation.

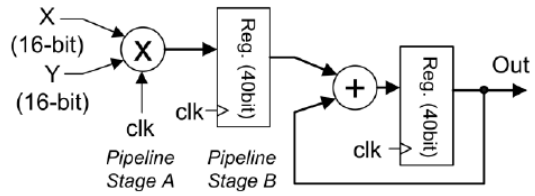

Figure 7: Regular MAC unit [12]

In reference paper [13], a new architecture of a multiplier-squarer is proposed using MAC units. This new architecture helps in area reduction by 11.23% of MAC unit when compared with conventional squarer and increase computation speed [12, 13].

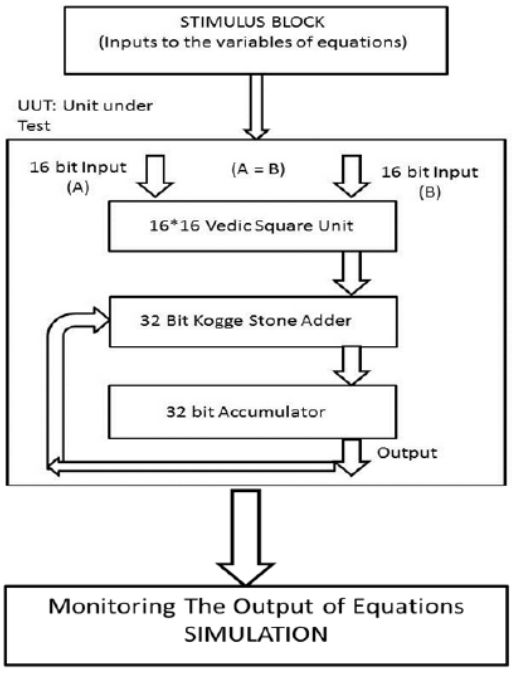

Figure 8: Proposed Architecture in [12, 13]

III. CONCLUSION

We have seen different implementations for MAC unit for various applications. But the high demand of MAC unit is in Digital signal processing field. Basically it provides hardware support for number of DSP applications. It also supports signed/unsigned integers plus signed fixed-point fractional input operands. Fused MAC unit executes faster than basic MAC unit. The use of MAC unit in DSP applications is not limited upto multiplication and addition but it performs well the division, squares, and square-root operations also. It can be used in digital filters. A huge amount of data needs to be transferred quickly affects the throughput in DSP applications. But the data can be transferred with the help of MOVEM instruction.

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