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Implementation of 5-level Flying Capacitor Multi Level Inverter

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Abstract –**This research work is for comparison of two different topologies of multi-level inverters (Diode clamped inverter and Flying capacitor clamped inverter). The multilevel inverter considered here is 5-level inverter. This comparison is done with respect to Total Harmonic Distortion (THD) only, i.e. the voltage and current harmonic contents both kind of topologies will be compared. For each inverter, IGBTs or MOSFETs can be used as switching devices to make the comparisons more accurate. The switches that are used for different inverters are the same for all of the inverters. Each inverter is controlled by the multi-carrier sinusoidal pulse width modulation (SPWM). The comparative results of the harmonic analysis have been obtained in MATLAB/SIMULINK.**

Keywords – **FCMLI, PWM, SPWM, THD.**

I. Introduction

During the last decades, renewable energy resources have become an important part of the worldwide concern with clean power generation. However, due to the variable nature of renewable energy sources, output voltage and frequency adjustments are the challenging issues to connect these systems to power grids or to enable different applications. Various families of power electronic inverters have been designed to comply with the requirements of renewable energy systems.

In response to the demand for medium and high power applications, new power inverter topologies and new semiconductor technology to drive all needed power have been released. The development of high voltage and current power semiconductors to drive high power inverter systems is continuing. From a practical point of view, multilevel inverters are suitable configurations for the high power applications in which high output voltage using medium voltage devices can be generated. Besides this focal characteristic, multilevel inverters present high quality performance due to the generation of a stepped output voltage which is closer to the sinusoidal waveform which allows reduction in harmonic contents of the output signal and, eventually, the size of the output filter.

Although each type of multilevel inverter shares the advantages of multilevel voltage source inverters, they may be suitable for specific applications due to their structures and drawbacks. Two well-known topologies of multilevel inverters, diode-clamped and cascade are widely used in renewable energy applications due to their structures. However, before the quality of these kinds of inverters can be enhanced, some problems need to be overcome. These problems have become the focus of this research work and are explained below. Basically, diode-clamped multilevel inverters synthesize a small step of staircase output voltage from several series levels of DC link capacitor voltages. This structure has advantages in power inverters and renewable energy systems. However, it experiences a capacitor imbalance for certain operating conditions in terms of modulation index (MI) and load power factor (PF) which can cause unequal DC link capacitor voltages. The unbalanced capacitor voltages lead to a disturbance in output voltage which can damage the switching components and cause an undesirable distortion at inverter output. There are some topologies and control algorithms for capacitor voltage balancing; however, these increase the complexity and cost of the control system and are not applicable in all conditions. Thus, there is no mature topology for a wide range of operations for more than three-level inverters. From this circumstance, Problem-1 arises:

Problem-1: The capacitor voltage imbalance problem in diode-clamped inverters

To remedy this problem, different control methods and circuit topologies are investigated and evaluated with respect to complexity of control, practical operation points of the inverter, and cost of the system. In order to compare the different topologies and control methods, selected topologies have been targeted in state of the art renewable energy applications. DC-DC inverters are usually utilized as front-end inverters in renewable energy systems to supply inverters' DC link voltage. Therefore, capacitor voltage balancing can be addressed from

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the DC-DC side, instead of from the inverter side. This factor has inspired the first part of this thesis (and the exploration of the first research problem) to focus on developing the new generation of economic DC-DC inverters specifically for renewable energy systems.

Multilevel inverters offer many attractive advantages for high and medium power applications; however, the output waveform quality is still a challenging issue due to the complexity of structures and the control strategy of these inverters. This extra complexity sometimes limits the opportunity to introduce high power quality, high efficiency and fault-tolerant operation as these are proportional to the number of power components. Therefore, increasing the number of output voltage levels to enhance the quality of output waveforms can create extra cost and increase the complexity of the physical layout and control of the system. This leads to Problem-2:

Problem-2: To revise the configuration of multilevel configurations used in renewable energy systems, such as diode-clamped and cascade inverters, to increase the number of voltage levels with a minimum number of components.

Various Pulse Width Modulation (PWM) techniques and design issues of asymmetrical DC link arrangements for multilevel inverters are taken into account to present an optimum design for maximum output resolution, with a minimum number of components and losses.

The main objective of this paper is to implement Flying Capacitor Multi Level Inverter. A 5- level Capacitor-clamped multilevel inverter circuit model is proposed. The comparative results of the harmonic analysis have been obtained in MATLAB / SIMULINK.

II. Multi-Level Inverters

Multi-level inverters are combinations of semiconductors and voltage sources that provide an output voltage above the unit ratings of each switch and an apparent frequency greater than the switching frequency of each switch [4].

In general, multi-level voltage inverters can be seen as voltage synthesizers, in which the output voltage is synthesized from several levels [18]. The most important advantages of multi-level topology by compared to the conventional two-level topology are [19]:

- The output voltage is scaled with at least three voltage levels and therefore has a better frequency spectrum. As a result, the necessary filter elements are smaller and less expensive.
- Using higher output voltages increases the power of the inverter without increasing the current.
- Increasing the apparent output frequency allows higher system dynamics.

However, these inverters also have some disadvantages:

- As voltage levels increase the control structure becomes more complex.
- Problems of capacitor voltage imbalances appear.

A review of publications in recent years shows us that the study of multi-level inverters (topology analysis, control, modulation, etc.) is now one of the most important topics in power electronics.

The development of multi-level technology has been marked by two factors. On the one hand, the technological evolution of semiconductor materials allows the realization of higher power and voltage inverters. On the other hand, even though the control of multi-level inverters is complicated, the evolution of digital signal processors with high computing capacity and very fast reaction speed and low cost made it possible to implement this control [20].

It should be noted that the choice of the best multilevel topology and the best control or control strategy for each given application is often not easy to find [21].

This paragraph is intended to introduce the general principle of multi-level behaviour. Figure 1 helps to understand how multi-level inverters work. A two-level inverter is shown in Figure 1(a), in which the semiconductor switches have been replaced by an ideal switch. The output voltage can only take two values: 0 or E. In Figure 1(b), the output voltage of three levels can take three values: 0, E or 2E. In Figure 1(c) the general case of n levels is presented [3] [22].

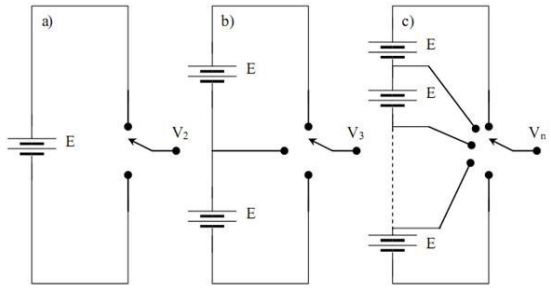

Figure 1: Multi-level inverter [3]

In Figure 1:
(a) At two levels
(b) At three levels
(c) n levels

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Increasing the number of the level makes it possible to improve the waveforms at the output of the inverter, particularly in terms of harmonic content, but this requires a much more complex control and a large number of semiconductors used. This makes the overall system more expensive and especially more complex.

III. Proposed Methodology

A. Flying Capacitor Multi Level Inverter Structure

The capacitor clamped inverter alternatively known as flying capacitor was proposed by Meynard and Foch in 1992 [29]. The structure of this inverter is similar to that of the diode- clamped inverter except that instead of using clamping diodes, the inverter uses capacitors in their place. The flying capacitor involves series connection of capacitor clamped switching cells. This topology has a ladder structure of dc side capacitors, where the voltage on each capacitor differs from that of the next capacitor. The voltage increment between two adjacent capacitor legs gives the size of the voltage steps in the output waveform. Figure 2 shows the five-level capacitor clamped inverter.

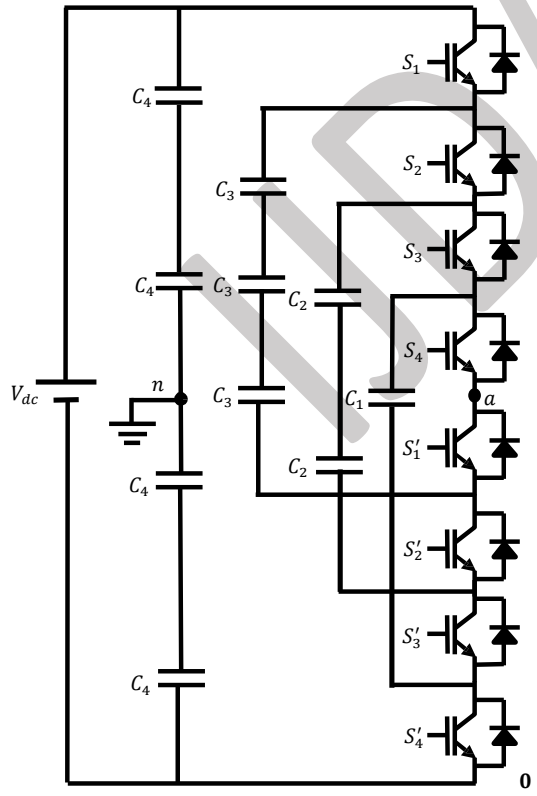

Figure 2: 5-level Capacitor-clamped multilevel inverter circuit topology

B. Operation of FCMLI

In the operation of flying capacitor multi-level inverter, each phase node (a, b, or c) can be connected to any node in the capacitor bank. Connection of the a-phase to positive node V_3 occurs when S_1 and S_2 are turned on and to the neutral point voltage when S_2 and S_1' are turned on. The negative node V_1 is connected when S_1' and S_2' are turned on. The clamped capacitor C_1 is charged when S_1 and S_1' are turned on and is discharged when S_2 and S_2' are turned on. The charge of the capacitor can be balanced by proper selection of the zero states. In comparison to the three-level diode-clamped inverter, an extra switching state is possible. In particular, there are two transistor states, which make up the level V_3. Considering the direction of the a-phase flying capacitor current I_a for the redundant states, a decision can be made to charge or discharge the capacitor and therefore, the capacitor voltage can be regulated to its desired value by switching within the phase. As with the five-level flying capacitor inverter, the highest and lowest switching states do not change the charge of the capacitors. The two intermediate voltage levels contain enough redundant states so that both capacitors can be regulated to their ideal voltages.

Similar to the diode clamped inverter, the capacitor clamping requires a large number of bulk capacitors to clamp the voltage. Provided that the voltage rating of each capacitor used is the same as that of the main power switch, an N level inverter will require a total of $(N-1)*(N-2)/2$ clamping capacitors per phase in addition to the $(N-1)$ main dc bus capacitors.

Unlike the diode-clamped inverter, the flying-capacitor inverter does not require all of the switches that are on (conducting) in a consecutive series. Moreover, the flying-capacitor inverter has phase redundancies, whereas the diode-clamped inverter has only line-line redundancies {1, 3}. These redundancies allow a choice of charging / discharging specific capacitors and can be incorporated in the control system for balancing the voltages across the various levels.

Voltage synthesis in a five-level capacitor-clamped inverter has more flexibility than a diode-clamped inverter. Using Figure 5.1 as the example, the voltage of the five-level phase-leg 'a' output with respect to the neutral point n (i.e. V_{an}), can be synthesized by the following switch combinations.

1. Voltage level $V_{an} = V_{dc}/2$, turn on all upper switches $S_1 - S_4$.
2. Voltage level $V_{an} = V_{dc}/4$, there are three combinations.

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a. Turn on switches S_1, S_2, S_3 and S_1'. ($V_{an} = V_{dc}/2$ of upper $C_4's - V_{dc}/4$ of $C_1's$).
b. Turn on switches S_2, S_3, S_4 and S_4'. ($V_{an} = 3V_{dc}/4$ of upper $C_3's - V_{dc}/2$ of $C_4's$).
c. Turn on switches S_1, S_3, S_4 and S_3'. ($V_{an} = V_{dc}/2$ of upper $C_4's - 3V_{dc}/4$ or $C_3's + V_{dc}/4$ of upper C_2').

3. Voltage level $V_{an} = 0$, turn on upper switches S_3, S_4 , and lower switch S_1', S_2'.
4. Voltage level $V_{an} = -V_{dc}/4$, turn on upper switch S_1 and lower switches S_1', S_2' and S_3'.

Voltage level $V_{an} = -V_{dc}/2$, turn on all lower switches S_1', S_2', S_2' and S_3'.

IV. Simulation And Results

The performance of proposed algorithms has been studied by means of MATLAB simulation.

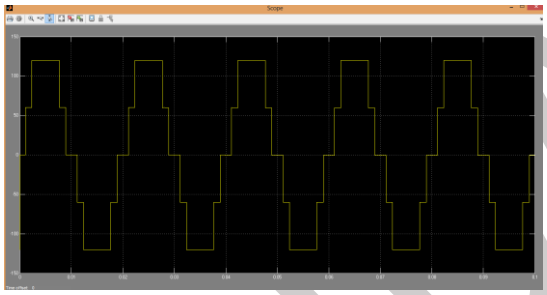

Figure 3: Voltage waveform of five level flying capacitor clamped inverter

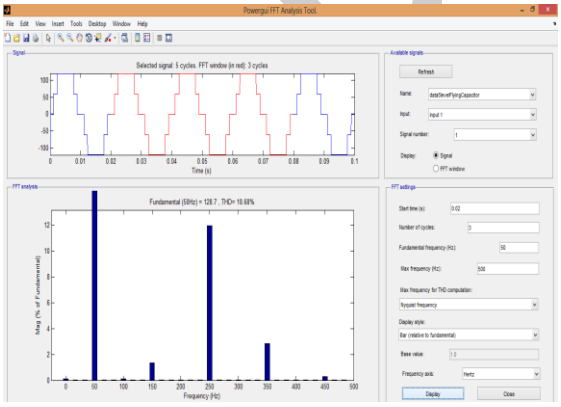

Figure 4: Total Harmonic Distortion of voltage waveform of five level flying capacitor clamped inverter

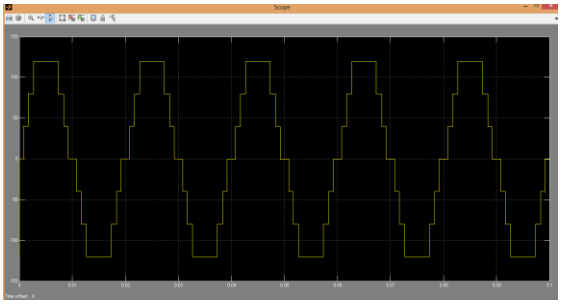

Figure 5: Voltage waveform of seven level flying capacitor clamped inverter

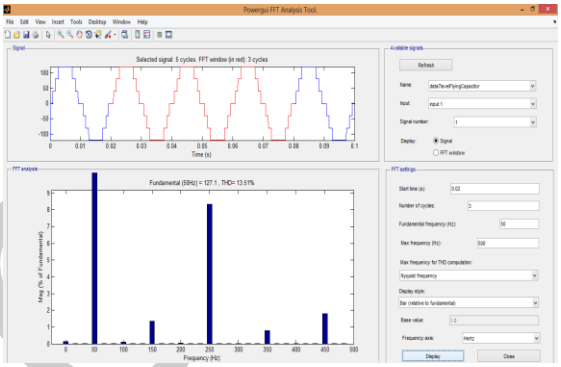

Figure 6: Total Harmonic Distortion of voltage waveform of seven level flying capacitor clamped inverter

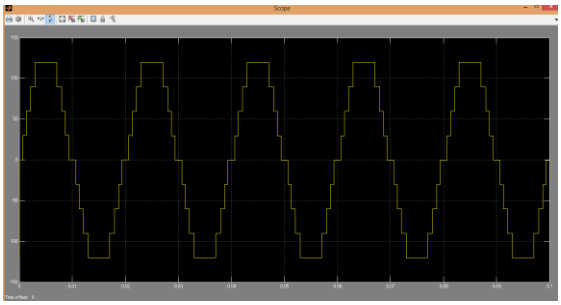

Figure 7: Voltage waveform of nine level flying capacitor clamped inverter

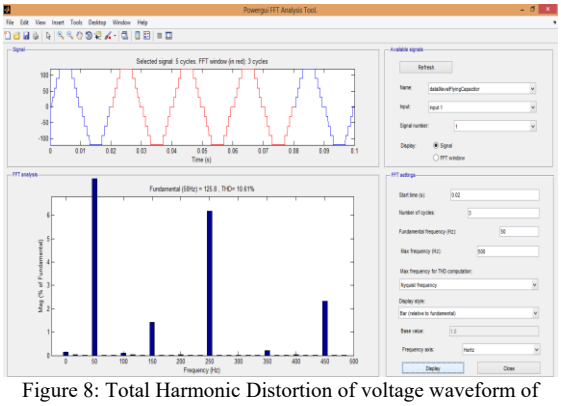

Figure 8: Total Harmonic Distortion of voltage waveform of nine level flying capacitor clamped inverter

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V. CONCLUSION

The work carried out and described in this paper work aimed at contributing to the improvement of the performance of the multilevel diode-clamped and flying capacitor clamped inverters, the control of this topology generates a higher complexity in the control algorithms since the maintenance of the voltages across the capacitors is an additional constraint to satisfy to ensure correct conversion and good quality. The presented solution uses the use of auxiliary circuits dedicated to the balancing of voltages. The inverter is therefore very interesting for renewable energy conversion systems, because it increases the efficiency, while maintaining a stable dynamic under the effect of a non-linear or unbalanced load. Experimental test results of the proposed technique were given and compared to those of the simulation. It is found that the total harmonic distortion is reduced with the increase of voltage level.

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